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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/009,051	04/22/2002	Stefan-Horea Culca	20798/0204662-US0	4397

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EXAMINER

LUGO, DAVID B

ART UNIT	PAPER NUMBER
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2611

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/009,051

Applicant(s)

CULCA, STEFAN-HOREA

Examiner

David B. Lugo

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21 is/are allowed.
- 6) ☒ Claim(s) 10-16, 18 and 20 is/are rejected.
- 7) ☒ Claim(s) 17 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/6/06 have been fully considered but they are not persuasive.

Regarding the rejection of claim 1, Applicant argues that Spracklen fails to teach a first circuit part including “a first transmitter circuit part connected to a first transmitter terminal of the first unit [and] a first receiver part connected to a first receiver terminal of the first unit.” The Examiner respectfully disagrees. While the Spracklen discloses a single-byte input/output port P for communication between the interface and a resident computer, the interface is considered to be part of the recited “first unit.” Figures 4A-4C disclose details of the interface, where the interface includes a first transmitter circuit part in Figure 4B connected to a first transmitter terminal TXD, and a first receiver circuit part in Figure 4C connected to a first receiver terminal RXD. All of these elements are part of the first unit, since they are part of the interface which is considered to be part of the first unit. Thus, Spracklen clearly discloses the aforementioned claim limitations.

Applicant further argues that the combination of Spracklen and Price fail to teach or suggest “a first signal state of the first receiver terminal is capable of being changed as a function of a signal state of the second transmitter terminal.” The Examiner respectfully disagrees. As indicated in the previous Office action, Spracklen discloses that when data is to be transmitted, the transceiver is in a SYNC WAIT state while it checks to see if the channel is IDLE (see state diagram - Fig. 3A). If the channel is not IDLE (i.e. the channel is in a packet-being-transmitted

Art Unit: 2611

state meaning the other transceiver is in a PACKET state), then the transceiver remains in the SYNC WAIT state, otherwise it moves to the PACKET state.

Applicant also states that there is no indication that the input/output port P changes signal state as a function of data on the channel, because the signal state of the input/output ports of P is not synchronous with the signal state of the terminals TXD and RXD. However, as indicated above, terminals TXD and RXD are considered to correspond with the claimed “first transmitter terminal” and “first receiver terminal” respectively, not the input/output port P. Therefore, Spracklen is considered to teach the recited claim limitation.

Applicant also argues that the combination of Spracklen and Price is improper, as Price teaches away from a second circuit part being interconnectable to a first circuit part via a reference potential line. However, Price clearly shows in Figure 4 a first circuit part connected with a second circuit part via a reference potential line (i.e. ground). While Price states that capacitors are used to by-pass each of the supply voltages to ground and to by-pass the supply voltages to each other, this configuration is shown in Figure 5, where the ground plane is shown to be intact. It is also noted that the presence of elements coupled between a transmission line connecting a first transceiver unit with a second transceiver unit does not mean that the first and second transceivers are not connected, as the term connected does not preclude insertion of various elements in the path.

Accordingly, the rejection of claims 10-16, 18 and 20 is maintained and is restated below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2611

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 10-16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spracklen et al. U.S. Patent 4,337,465 in view of Price et al. U.S. Patent 5,736,796.

Regarding claim 10, Spracklen discloses a data transmission system comprising a first unit or transceiver communicating with a second unit or transceiver (i.e. nodes 11 – Fig. 1), where each unit includes an interface having a transmitter circuit part connected to a transmitter terminal (TXD) as shown in Figure 4B, and a receiver circuit part having a receiver terminal (RXD) as shown in Figure 4C, where the unit transmits and receives data over the transmission line via terminals TXD (Fig. 4B) and RXD (Fig. 4C), respectively, for communicating with other transceivers, and where the transceivers are connected to each other via the transmission line, as shown in Figure 1. Spracklen further shows a current source, shown in Figure 7, that feeds current into the transmission line (col. 7, lines 16-18) so that a first signal state of the receiver of the first circuit part (i.e. SYNC WAIT state) is capable of being changed as a function of a second signal state of the transmitter of second circuit part (i.e. PACKET state), and a third signal state of the receiver of the second circuit part (i.e. SYNC WAIT state) is capable of being changed as a function of a fourth signal state of the transmitter of first circuit part (i.e. PACKET state), as Spracklen discloses that when data is to be transmitted, the transceiver is in a SYNC WAIT state while it checks to see if the channel is IDLE (see state diagram - Fig. 3A), and if the channel is not IDLE (i.e. the channel is in a packet-being-transmitted state meaning the other transceiver is in a PACKET state), then the transceiver remains in the SYNC WAIT state, otherwise it moves to the PACKET state. Further, the second transceiver (second circuit part)

Art Unit: 2611

operates in a complementary fashion. Spracklen does not expressly show terminals at each circuit part for a reference potential line.

Price discloses a communication system in Figure 4 where two communication units are connected via a transmission line 72 and a reference potential line (i.e. GND). It would have been obvious to one of ordinary skill in the art to employ the teachings of Price of using a reference potential line in the system of Spracklen in order to provide a common path to ground, as is well known in electrical circuit design.

Regarding claim 11, each of the transceivers is described as being associated with a resident computer (col. 5, lines 25-27), where the computer inherently includes a display and a processor, and further includes an operating control unit (bus control 21 – Fig. 4A), and a plurality of signal inputs and outputs as shown in Figures 4A-4C. Spracklen does not expressly state that the components are disposed in a common housing. However, it is well known in the art to provide components in a single housing to reduce the length of the lines connecting the components. Therefore, it would have been obvious to one of ordinary skill in the art to implement the components in a common housing in order to reduce the length of the lines connecting the components thereby eliminating noise associated with long transmission lines.

Regarding claim 12, it is well known in the art for computers to include processing units having microcontrollers. It would have been obvious to one of ordinary skill in the art to use microcontrollers in the computers of Spracklen as a matter of design consideration.

Regarding claim 13, the transceiver is described as being associated with a resident computer (col. 5, lines 25-27), where the computer inherently includes a display and a processor, and further includes an operating control unit (bus control 21 – Fig. 4A), and a plurality of signal

Art Unit: 2611

inputs and outputs as shown in Figures 4A-4C, wherein the second transceiver is considered to expand a function of the first unit. Spracklen does not expressly state that the components are disposed in a common housing. However, it is well known in the art to provide components in a single housing to reduce the length of the lines connecting the components. Therefore, it would have been obvious to one of ordinary skill in the art to implement the components in a common housing in order to reduce the length of the lines connecting the components thereby eliminating noise associated with long transmission lines.

Regarding claim 14, it is well known in the art for computers to include processing units having microcontrollers. It would have been obvious to one of ordinary skill in the art to use microcontrollers in the computers of Spracklen as a matter of design consideration.

Regarding claim 15, Spracklen shows in Figure 7 that the current source is integrated in the unit.

Regarding claim 16, Spracklen shows in Figure 7 that the transceivers include a semiconductor switch (transistor 55).

Regarding claim 18, Spracklen states that the current source is a constant current source (col. 7, lines 16-19).

Regarding claim 20, Spracklen shows in Figure 7 that the current source includes an ohmic resistor 57 connected to a supply potential 56 with a first end, and to the data transmission line via transformer 44 with a second end thereof.

Allowable Subject Matter

4. Claims 17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
5. Claim 21 is allowed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

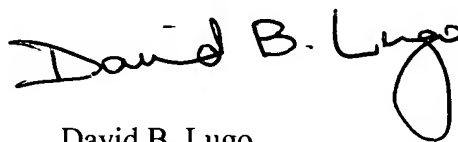
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2611

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink that reads "David B. Lugo". The signature is fluid and cursive, with the last name "Lugo" having a large, looping tail.

David B. Lugo
Patent Examiner

2/28/07